Design of an FPGA-Based OFDM-STBC Transceiver for WiMAX 802.16e Standard

Sugondo Hadiyoso
Telkom Applied Science School
Telkom University
Bandung, Indonesia
sgo@ittelkom.ac.id

Rina P. Astuti
Electrical and Communication Department
Telkom University
Bandung, Indonesia
rina_pudjiastuti@yahoo.com

Iswahyudi Hidayat
Electrical and Communication Department
Telkom University
Bandung, Indonesia
isw@ittelkom.ac.id

Abstract—**One of the wireless communication technologies, especially Broadband Wireless Access (BWA) is Worldwide Interoperability for Microwave Access (WiMAX). WiMAX communication system tend to use OFDM and MIMO systems in order to provide high data rates, minimizing bandwidth and fading effects. This work presents the design and implementation of OFDM with 512 subcarriers and 2x2 STBC MIMO transceiver for WiMAX 802.16e standard. The design consists of (Space Time Block Code) STBC, Fast Fourier Transform (FFT / IFFT) for subcarrier division, mapping and de-mapping symbols, and system integration using high level design tool based on VHSIC *Hardware Description Language* (VHDL) on FPGA. Module is targeting on a specific Kintex 7 XC7K325T-FBG900 FPGA. Since the module implemented and tested, bits are received in ideal conditions (no noise) is no error. Bit rate is attained 28,3 Mbps for operating frequency clock of FPGA 100 MHz. Refer to the WiMAX 802.16e standard which needs minimum data rate is 4 Mbps, this system can be applied. OFDM-STBC module require around 1-9 % of the available logic memory resource.**

Keywords—WiMAX, OFDM, MIMO, STBC, FFT/IFFT, VHDL, FPGA

I. INTRODUCTION

In modern communication services, data rate, bandwidth used, the bit error rate (BER), are parameters that is considered to produce a reliable wireless communication system. Many systems have been proposed and OFDM combined with MIMO system has gained much attention to solve that problems. OFDM technique was first developed in 1960s and nowadays OFDM used for the communications device that requires high data rate [1].

Basic communication system using OFDM consists of a mapping/de-mapping (PSK or QAM), serial to parallel, parallel to serial converter and a FFT / IFFT processor. In this work added to the system by implementing STBC MIMO 2x2 is intended to support the WiMAX 802.16e standard. In this work added MIMO system by implementing STBC 2x2 to support the WiMAX 802.16e standard. STBC system is used to increase the data rate and bandwidth efficiency.

There are some methods to implementation of the STBC-OFDM system at the level of Intermediate Frequency (IF) or digital domain. The first one is using ASIC (Application Specific Integrated Circuit). ASICs are the fastest, smallest, and lowest power way to implement OFDM into hardware. The main problem using this method is inflexibility of design process involved and the longer time to market period for the designed chip [2].

FPGA (Field Programmable Gate Array) is the second method for STBC-OFDM system implementation. FPGA is a programmable logic device to support the implementation of logic circuits which require large of memory. The advantage of using FPGAs is reducing board area, reduce power consumption, reduce costs, increase speed and FPGA systems are a part of the ASIC. Build the system using FPGA compared to ASIC, more flexible for reconfiguration as Mentioned in [3].

Another method to implement OFDM-STBC system is using a microprocessor or microcontroller. But it has limited memory and speed when compared to FPGA or ASIC so that it will be difficult and inefficient if it is used for system implementation.

Many methods can be performed to obtain OFDM with good performance in accordance with the purpose of implementation as well as the STBC system. However, the challenges the implementation is getting minimum resource memory utilities but the system remains reliable. In the project research that has been done before, especially the design of the FFT/IFFT processor in OFDM transceiver[4,5-6,7-8] generally use radix-2 algorithms which has a weakness, if the number of points of FFT/IFFT become large then the stage of the calculation becomes more complex, so when applied to FPGA requires more logic memory in FPGA. Using radix-8 algorithm can reduce calculation complexity of FFT/IFFT so it can reduce memory usage on the FPGA.

Lenin Gopal [2] designs OFDM transceiver for DVB-T standard on FPGA that consists of QPSK modulator/demodulator, IFFT/FFT module. Gopal investigated the effects of using the number of bit representation for power spectral density. Manoto [9] made FFT 512 point designed on FPGA but there is a problem in the FFT module and the validation process is performed at the level of simulation.

In this research focused on the implementation of OFDM-STBC at the level baseband processing for WiMAX 802.16e standard. The work consist of the mapping/de-mapping symbol, serial to parallel, parallel to serial, encoder/decoder

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STBC, and the IFFT / FFT processor is implemented on the FPGA Kintex 7 chip.

The main contents is organized as follows, section II presents a description of the WiMAX 802.16e standard, STBC, and OFDM fundamentals. At section III is brief description of the system design. Test results are described in section IV and conclusions at section V.

II. WIMAX, OFDM & STBC OVERVIEW

A. The WiMAX 802.16e Standard

One of the wireless communication technologies, especially Broadband Wireless Access (BWA), which supports high data rate communication services in high mobility conditions, is Worldwide Interoperability for Microwave Access (WiMAX). The system is released by the Institute of Electrical and Electronics Engineering (IEEE) has reliability for communications: Local Area Network (LAN) and mobile communication technologies. The first time, in 2001 has released the 802.16 standard then improved in 2004 become 802.16a standard is called fixed WiMAX. In December 2005, the IEEE group completed and approved IFEEE 802.16e-2005, which is improvement of the previous standard that added mobility support [10] and 802.16e standard then called as mobile WiMAX.

This project based on mobile WiMAX standard because of mobile WiMAX development which is predicted to be widely used by the user since it is more flexible and high mobility. The referenced parameters in this project are shown in table 1.

Table 1. WiMAX 802.16e Standard

Parameter	802.16e
Multiple Access Method	S-OFDMA
Bandwidth Supported	1.25/2.5/5/10/20
	1.75/3/3.5/5.5/7
FFT Size	128/256/512/1024/2048
Channel Code	Concatenated Convolutional RS
	code, Block TC, CTC, LDPC
AAS (Advance Antenna System)	Yes
STC Support	2/3/4 Antennas
Modulation	QPSK, 16 QAM, 64 QAM

Standard parameter for mobile WiMAX that is used in this research are FFT point, modulator/demodulator QPSK and STBC 2x2 for support 2 antennas system.

B. OFDM Fundamentals

OFDM is a special form of multicarrier modulation (MCM), where a single data stream is transmitted over a number of lower rate subcarriers which are orthogonal between subcarriers. This orthogonal effect can make overlapping among subcarriers without inter-carrier interference (ICI). OFDM system employs the IFFT and FFT for making orthogonal frequency [11]. Transceiver block of OFDM is shown in Fig. 1.

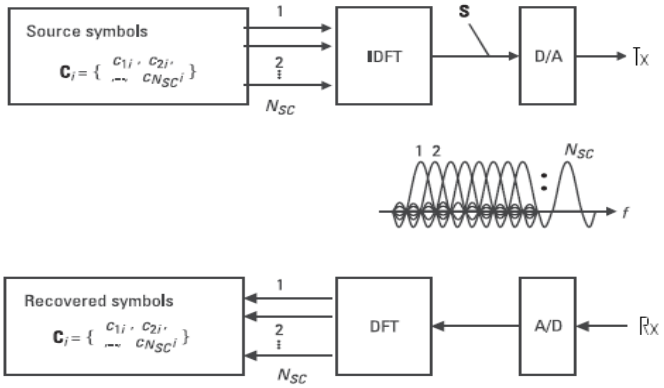

Fig. 1. Tranceiver block diagram for the OFDM [11]

C. STBC Alamouti Fundamentals

The scheme uses two transmit antennas and two receive antennas. In Fig. 2, the encoding is done in space and time (space–time coding). The encoding, however, may also be done in space and frequency. Instead of two adjacent symbol periods, two adjacent carriers may be used (space–frequency coding) [12].

$$\begin{array}{c} \\ t \\ t+1 \end{array} \begin{array}{c} \begin{array}{cc} T_{x0} & T_{x1} \end{array} \\ \begin{bmatrix} S_0 & S_1 \\ -S_1^* & S_0^* \end{bmatrix} \end{array}$$

Fig. 2. Alamouti Scheme [12].

III. SYSTEM DESIGN

The stages of implementation to complete the project are: Designs transceiver blocks system, design and simulation OFDM-STBC using MATLAB, design and simulation in Modelsim, finally implementation and testing on FPGA board.

In this work divides the design into two subsystems. At the transmitter side: QPSK for symbol mapping, STBC encoder, IFFT. The receiver consists of an FFT, STBC decoder and the QPSK slicer.

This system uses 100 MHz clock frequency generated by FPGA's differential clock. Each block of subsystems use 16 bit fixed point representation. In the following sections, each section subsystems are described in detail.

A. SIGNAL GENERATOR

Input data are generated bit stream by data generator which value is repeated every 16 bits. The tested data are [1 0 0 1 0 0 0 1 1 1 1 0 0 0 0 1].

B. *QPSK Mapping/De-Mapping*

Data bits from the signal generator will be formed into complex data (real & imaginary) symbols based on QPSK modulation scheme and multiplied by a constant modulation *k* = 0707, shown in table 2.

Table 2. QPSK Mapping

Input Bit	Simbol Representation*0,707	Binary Representation
00	0,707 + 0,707 i	0,707 = 0000101101010000
01	0,707 – 0,707 i	
11	-0,707 – 0,707 i	-0,707 = 1111010010110000
10	-0,707 + 0,707 i	

QPSK De-mapping- in the symbol representation used a sign bit on the MSB, bit '1' indicates data bit = 1 and bit '0' indicates data bit = 0. So with this method is simple way to get information bits. This method is called a hard decision. Detail process is shown in table 3.

Table 3. QPSK De-Mapping

Real	Imajiner	Sign Bit		Data Bit
		Real	Imajiner	
0000101101010000	1111010010110000	0	1	[0 1]
1111010010110000	1111010010110000	1	1	[1 1]
1111010010110000	0000101101010000	1	0	[1 0]
0000101101010000	0000101101010000	0	0	[0 0]

C. *STBC*

STBC encoder uses two transmit antennas and two receive antennas based on Alamouti scheme already described in section II. STBC module consists of real and imaginary data processor because of FPGA can't compute the complex number from QPSK mapping module. The synthesis of STBC block in Modelsim is shown Fig. 3.

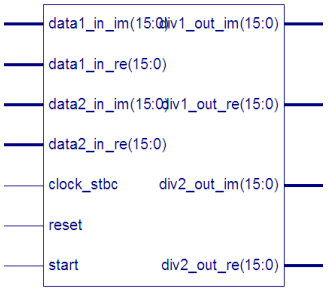

Fig. 3. STBC Encoder Block.

D. *IFFT/FFT*

In this project, implementation IFFT/FFT module is completed using radix-8 algorithm. This block consists of controller, addressing, RAM, ROM, twiddle factor, divider 512 dan 8-point FFT.

IFFT module based on FFT computation, by added multiplication process by a constant value (1/N point FFT) and change input arm. The system design of IFFT processor is shown in Fig. 4.

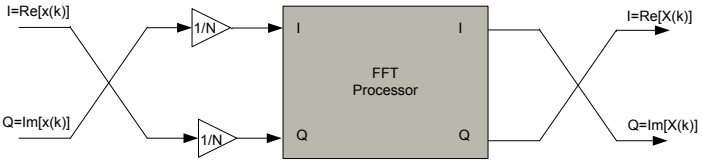

Fig. 4. IFFT Processor Block[9]

The results of hardware computation could be validated at MATLAB. The OFDM- STBC transceiver module implementation on FPGA are shown in Fig. 5

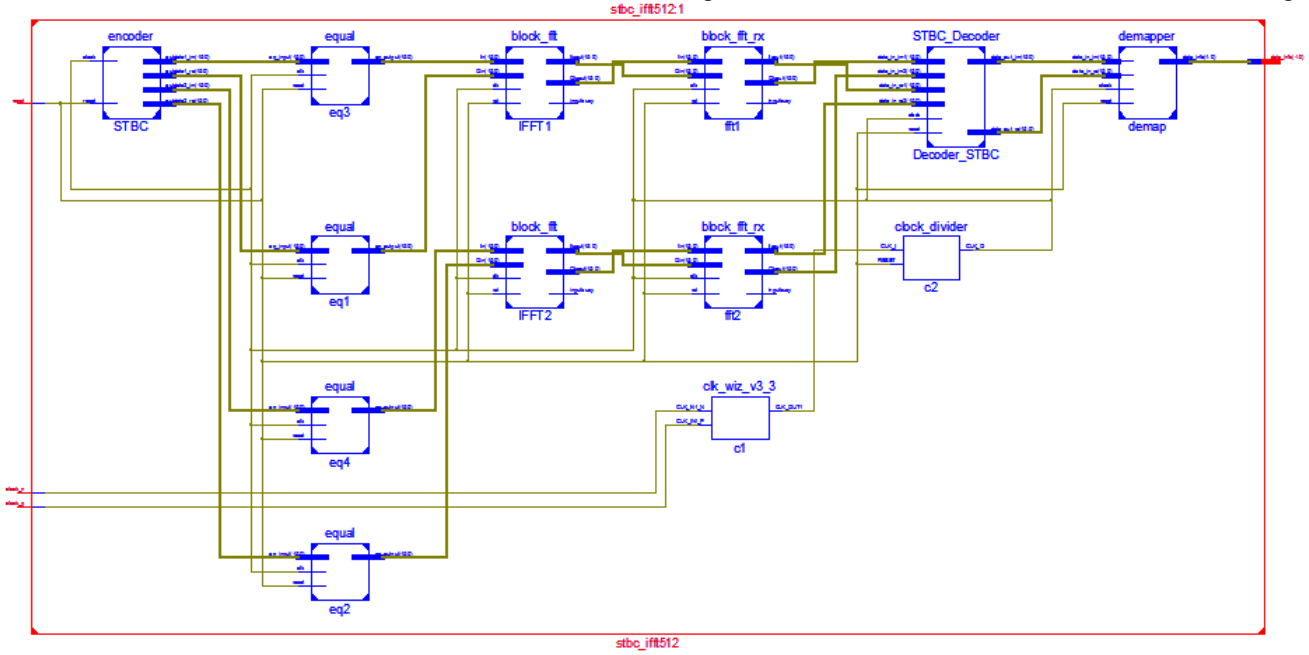

Fig. 5. RTL Schematic Design of OFDM-STBC Transceiver Modul

IV. RESULTS

Since the OFDM-STBC implementation and simulation is completed on high level design. Validation process is done by compare the output data among test bench, MATLAB, and FPGA.

The computation of IFFT/FFT is key success of the system design. In this part, the module possibility generating error due to mathematical process on binary data can make difference value between digital simulation and MATLAB.

The verification process is completed on simulation tool. Finally, module is targeting on a specific FPGA hardware. Hardware is tested by sending data bits itself in accordance with the format described in section III. The test results were observed at the receiver. The operating frequency used in this system is 100 MHz for all subsystems generated from internal clock. OFDM-STBC transceiver module is targeted to a Xilinx Kintex 7 board, from synthesis report STBC-OFDM modules require around 1-9% of the available resource. Design utilization resource that used is shown in Fig. 8. For additional information, implementation on FPGA is using Xilinx ISE Design Suite 13.2 software.

The Figure 6 shows the comparison of IFFT between the FPGA computation and MATLAB simulation. Results showed that the computation on FPGA is similar to the simulation in MATLAB and there are some differences but have small deviate values (Ave. Dev. =1.54). The comparison of FFT results between the FPGA computation and MATLAB simulation is shown in Table 4. There are differences due to rounding since binary data computation. This problem can resolved because of using QPSK mapping and hard decision method so information bits detected easily and correctly. Fig. 7 shows information bits which is sent and received. Table 5 shows device utilization memory of Kintex 7 FPGA.

Table 4. FFT Result

Point	FPGA		MATLAB	
	Real	Imag	Real	Imag
1	-3088	3402	-2896	2896
2	-2845.2	-2820.04	-2896	-2896
3	3391.7	3095.77	2896	2896
4	-3109.5	-3837.61	-2896	-2896
5	-3064.5	-3378.97	-2896	-2896
6	2838.3	2866.57	2896	2896
7	2743.3	3093.98	2896	2896
8	-2851.9	-2824.9	-2896	-2896
9	-3080.5	3414.49	-2896	2896
10	-2853.3	-2824.37	-2896	-2896
11	3384	3090.67	2896	2896
12	-3175.5	-3427.6	-2896	-2896
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
512	-2840.2	-2823.84	-2896	-2896

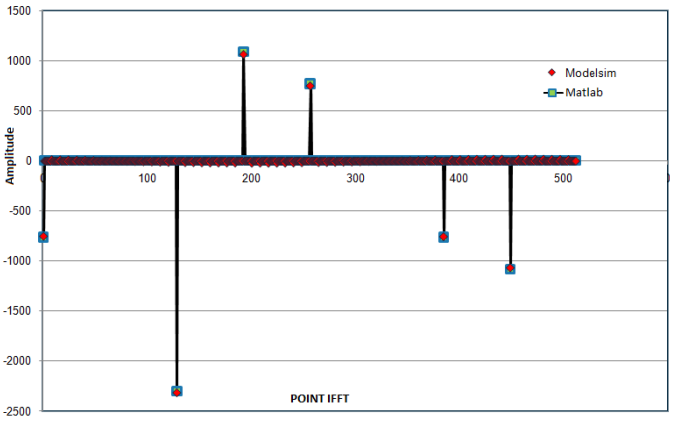

Fig. 6. Amplitude IFFT

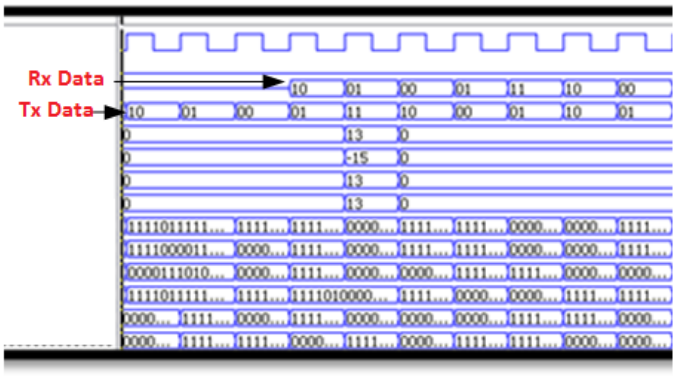

Fig. 7. Data Bit (Tx-Rx)

Table 5. Device Utilization Summary

Logic Utilization	Utilization
Number of Slice Registers	1%
Number of Slice LUTs	6%
Number of fully used LUT-FF pairs	9%
Number of bonded IOBs	1%
Number of Block RAM/FIFO	1%
Number of BUFG/BUFGCTRLs	3%
Number of DSP48E1s	7%

Total clock cycles required to process each 1024 information bits is 3607 clock cycles. Remember, this system using operation frequency of FPGA 100 MHz then the period is 10 ns. Based on the calculations below, bit rate is reached:

$$\text{Bitrate} = \frac{1}{36070\ ns} x\ 1024\ bit \approx 28{,}3\ \text{Mbps}$$

V. CONCLUSION

The FPGA based OFDM-STBC transceiver for WiMAX 802.16e standard has been implemeted on Kintex 7 XC7K325T-FBG900 FPGA. The challenges in implementing is getting minimum resource memory utilities but the system remains reliable has been achieved. This system using

operation frequency of FPGA 100 MHz, based on the calculations bit rate is attained 28,3 Mbps. Refer to the WiMAX 802.16e standard that used 5 MHz bandwidth which needs minimum data rate is 4 Mbps, this system can be applied. Data bits are received in ideal conditions (without noise) is no error although IFFT/FFT process can generate error computation, This problem can resolved because of using QPSK mapping and hard decision method so information bits detected easily and correctly. The OFDM-STBC transceiver module is targeted to an Xilinx Kintex 7, from sintesis report, OFDM-STBC module require around 1-9 % of the available resource. This research is expected to support the national industry in Indonesia to manufacture communication chips for WiMAX devices. The future work is to implement at radio frequency level, use more subcarrier for example 1024 or 2048, and integrated with channel encoder.

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