DESIGN AND IMPLEMENTATION OF LINEAR PRECODING LTE DOWNLINK BASED ON FPGA

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Abstract

The problem that often occur in multi-antenna wireless communication is how to maximize the throughput. Precoding is a generalization of beamforming to support multi-layer transmission in multi-antenna wireless communications. Beamforming is a signal processing technique used in sensor arrays for directional signal transmission or reception. In conventional single-layer beamforming, the same signal is emitted from each of the transmit antennas with appropriate weighting such that the signal power is maximized at the receiver output. When the receiver has multiple antennas, single-layer beamforming cannot simultaneously maximize the signal level at all of the receive antennas. Thus, in order to maximize throughput in a receiving antenna system, integrated precoding in multi-layer beamforming is required.

LTE linear precoding system for the transmitter side is built in this research. The precoding system will be built in VHDL code and will be implemented on FPGA. In this research, the precoding sistem consists of 64-QAM Mapper as input system, and will be connected to OFDM (IFFT) block. The precoding is built based on Transmission Mode (TM) 6 of LTE release 9 and will be using 3GPP codebook standard as the precoding matrix for TM 6 for 2x2 MIMO.

The research shows that by the used of linear precoding system in transmission, it decreases the complexion of detection system in precoding block on the receiver side. The implementation process shows that the research is implementable on hardware and will use 62% occupied slices, 11% slice register, and 27% of bounded IOBs resources of FPGA. with 2021 clock in total process, 121 clock in delay process and 1900 clocks to produce one OFDM symbol. The bitrate of the system is 161.68 Mbps.

Keywords: Linear precoding, codebook, FPGA, VHDL, MIMO

1. Introduction

Multimedia communications has developed rapidly for last decades. As multimedia communications become increasingly popular, mobile communications are expected to reliably support high data rate transmissions. The MIMO standard of LTE release 10[11] requires the precoding system to maximize the signal power in the receiver side. The previous has built the precoding scenario for 802.16e application in Matlab for simulation stage, but the work didn't implement the system on the hardware.[4] The other work has built only the mapper system for SISO (Single Input Single Output) system.[5] In this research, the precoding part is built and integrated with the previous works, the mapper and the OFDM part to make it closer to the LTE requirement for Transmission Mode 6 Scheme.

This research is expected to complete the precoding system of LTE 2x2 MIMO system by using linear precoding method which is completed by the use of codebook matrix. The precoder will be built in VHDL language and will be implemented on FPGA board.

2. Literature of Review

2.1 Precoding Transmission Mode in LTE Downlink

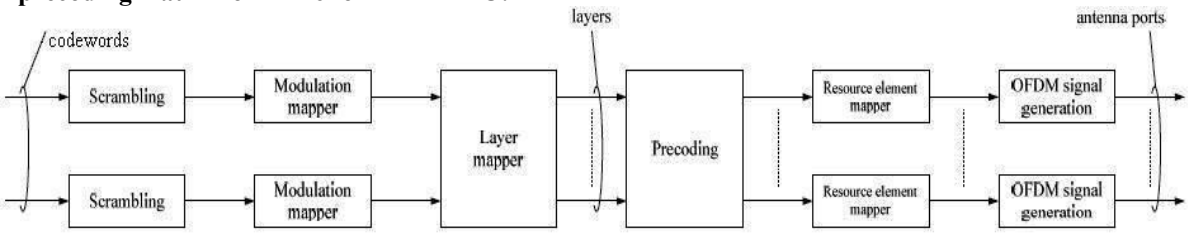

Figure 1. LTE Physical Layer

The mutiplication between transmitted symbol and precoding matrix is a way to overcome the rank defiency effect of channel matrix. Matrix channel rank deficiency is a condition where the channel coefficient value between transmitted anthenas practically uniform. This condition is a disadventage for MIMO detection. The good MIMO detection must be under full rank circumtances. Precoding does not change the channel coefficient (magnitude and phase), but it changes the magnitude and phase or even the number of the symbols that the symbols can compensate the rank deficiency of MIMO channel.

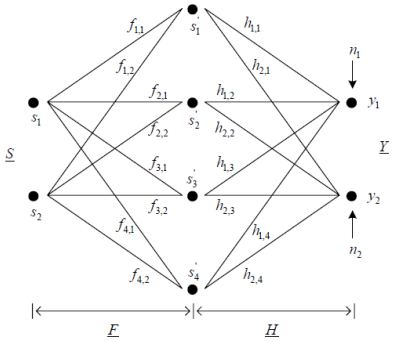

Figure 2. symbols, channel, and precoding correlation[4]

Symbol modification by precoder can be describes as below:

$$s_1' = f_{1,1}.s_1 + f_{1,2}.s_2$$
$$s_2' = f_{2,1}.s_1 + f_{2,2}.s_2$$
$$s_3' = f_{3,1}.s_1 + f_{3,2}.s_2$$
$$s_4' = f_{4,1}.s_1 + f_{4,2}.s_2$$

The idea of precoding is to use the channel knowledge on transmitter to adjust the tranmitted signal to the eigen structure of the channel matrix. Full gain of precoding is obtained by full Channel State Information (CSI). In FDD system, full CSI must be given by the receiver via feedback channel. This condition is not practical, because the bandwidth of the feedback channel is limited.[4]

This problem can be fixed using precoding system. The idea is the precoder is choosen from a set of limited precoding matrix called codebook, known to both transmitter and receiver side. The receiver chooses the optimal precoder from codebook as CSI function and sends the biner index of the matrix to the transmitter through limited feedback channel.

For the detection, Maximum Likelihood (ML) is the optimal detection algorithm, but ML is really complex to be implemented, however the linear receiver is sub-optimal, but less complicated in implementation. Optimal matrix precoding can be easily choosen based on specific selection criteria by simple calculation of the known codebook matrix.

3. Design of System

3.1 Modelling of Linear Precoding LTE

In the real LTE transmitter physical layer design, the precoding part consists of layer mapper, precoding, resource element mapper, and OFDM part. But in this research, the precoding part will be simplefied. The precoding part will be consist of the precoding and ofdm part. The layer mapper is not needed because this Research is working under the 6th sceme of Transmission Mode for LTE Release 9, where there is only one layer for the mapper. The resource element mapper part is also not included in this Research design.

The design of the precoding LTE will be shown as below:

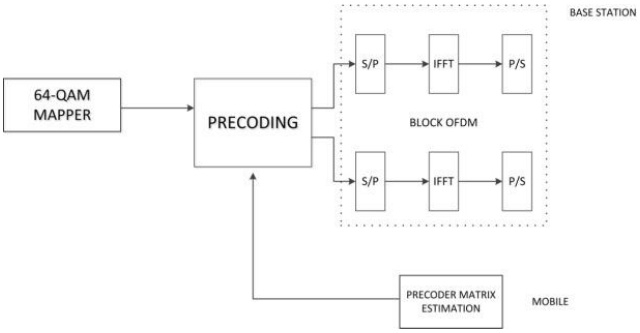

Figure 3. Precoding System Structure

3.2 Precoding Block

This research will design and implement the precoder for 6th shceme of Transmission Mode for LTE released 9 standard which is Closed-Loop Rank-1 Spatial Multiplexing for 2x2 antena case.

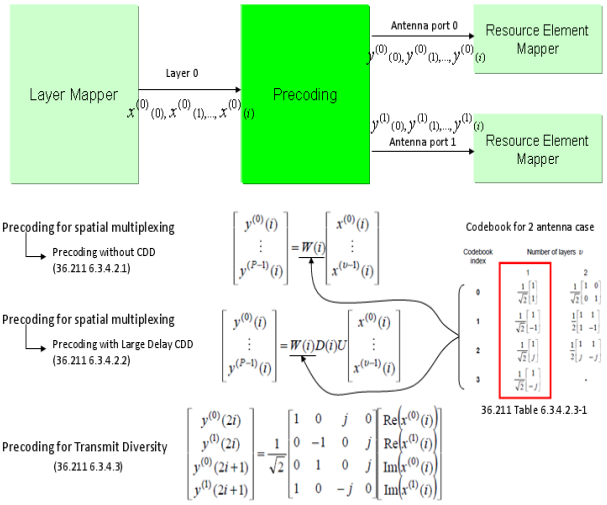

Figure 4. Transmission Mode 6 precoding procedure[13]

Table 3.1 Precoding/weighting for a 1-layer scenario using the codebook index[12]

Weights for 1 Layer			
Codebook index	**Matrix**	**Weights**	**Phase**
0	$\frac{1}{\sqrt{2}}\begin{bmatrix}1\\1\end{bmatrix}$	→ →	0^0
1	$\frac{1}{\sqrt{2}}\begin{bmatrix}1\\-1\end{bmatrix}$	→ ←	180^0
2	$\frac{1}{\sqrt{2}}\begin{bmatrix}1\\j\end{bmatrix}$	↑ →	90^0
3	$\frac{1}{\sqrt{2}}\begin{bmatrix}1\\-j\end{bmatrix}$	→ ↓	270^0

3.3 Precoding System Design in Xilinx

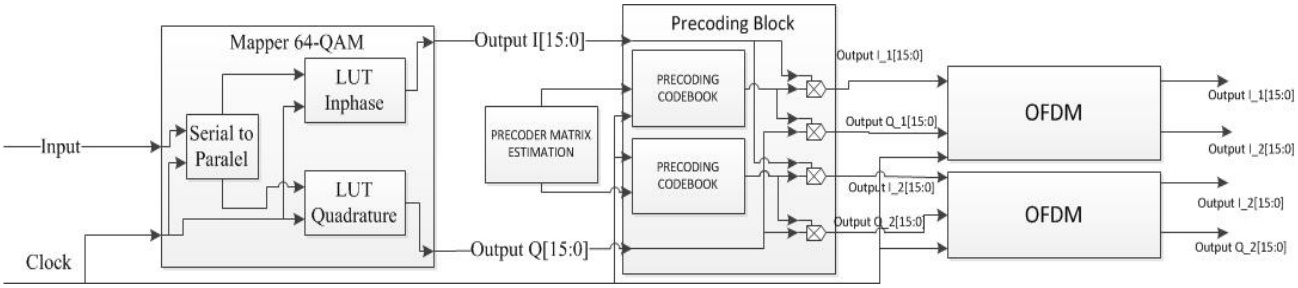

Figure 5. Precoding System Design in Xilinx

The precoding system will be consisted of three blocks which are the 64-QAM mapper, the precoding itself and the OFDM Block. Blocks syncronization will be using counter between each output that will be used as the next block input system and the next block.

First block is mapper block which will represent the input into 16-digit bit using almouti algorithm. The second block is the precoding block which works according to the received precoder matrix estimation, and the last block is the OFDM block using Cooley-Turkey FFT Algorithm in radix-8.

The input of the system will be in the form of bit stream which will be obtained by using input generator and the system is using universal clock as the controller of the system.

3.4 Precoding Block in Xilinx

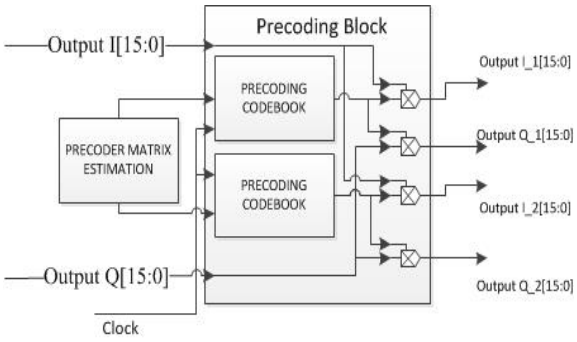

Figure 6. Precoding Block Design in Xilinx

The precoding block will get input from the previous block output. The precoding block works based on the precoder matrix estimation, where in reality is the feedback through feedback canal in LTE system which contain the channel information as the guide to choose the suitable precoding codebook for the transmitted signal. In this research, the precoder matrix estimation will be assumed beforehand and will be represented in 2-bit number which are 00, 01, 10, or 11. Every precoder matrix estimation will generate 2 precoding codebook value based on the 3GPP standard of precoding matrix.

The precoding codebooks will be choosen according to the received 2-bit precoder matrix estimation. The codebook value is also represented in 16-bit form which is listed as below.

Table 3.2 Precoder Matrix Estimation and the Precoding Codebook

Precoder Matrix	1st Precoding Codebook	2nd Precoding Codebook
00	0000101101010000	0000101101010000
01	0000101101010000	0000101101010000
10	0000101101010000	1111010010110000
11	0000101101010000	1111010010110000

After generating the codebooks, the codebooks will be multiplied with the mapped symbol from 64-QAM mapper and the output will be served as the input of the OFDM system. The multiplying process will generate two inphases and two quadratures output.

3.5 Precoding Block Simulation

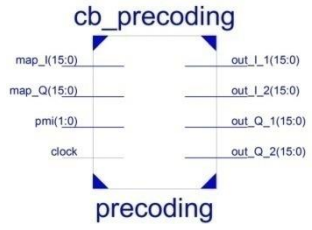

Figure 7. Precoding Block Schematic in Xilinx

The precoding block simulation is done using Isim on Xilinx and by comparing the data from manual calculation in saved in Microsoft Excel 2007 software.

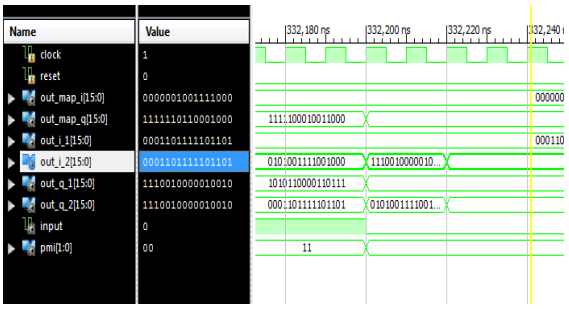

Figure 8. Precoding Block Simulation on Isim

4. Implementation and Analysis

4.1 Implementation of Precoding System on FPGA

FPGA for series Virtex-4 Xilinx XC4VLX25-SF363-12 with the spesification 64-MB DDR SDRAM, 32 bit interface running, clock oscillator 100 MHz, and other supported feature is used to

implement the designed LTE precoder system. The following picture is the picture of FPGA board that will be used in this research.

The flowchart of the implementation of system on FPGA board is shown below:

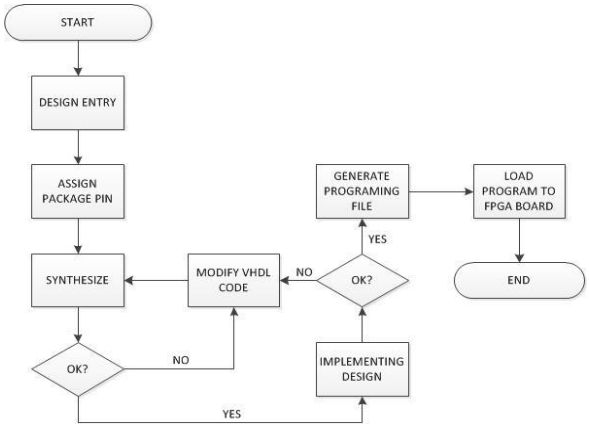

Figure 9. Flowchart of the implementation of system on FPGA board

4.2 System Implementation and Analysis

The implementation and the simulation stages show the same display of bit streams in the systems' output. It means that the designed system is implementable on the FPGA device. After implementation, the system specification is listed as below.

Table 4.1 Implementation specification

Mapper	64 QAM
MIMO Scheme	2x2
OFDM	512 subcarrier
Bit Rate	161.68 Mbps

Table 4.2 FPGA resource utility for Mapper-Precoder

Occupied slice	1%
Slice register	1%
4 input LUTs	1%
Bonded IOBs	27%
BUFG/BUFGCTRLs	6%

Table 4.3 FPGA resource utility for Precoder OFDM

Occupied slice	62%
Slice register	11%
4 input LUTs	48%
Bonded IOBs	27%
BUFG/BUFGCTRLs	9%

In the design of system and theoretical calculation, the precoding systems shows that even if all symbols combination and precoding codebooks multiplication suppose to generate 64x4 different symbols, but from the theoritical calculation, the precoder generates only 64x1 different symbols combination, which has the same value with total of symbols of the mapper, which are 64 symbols.

For every precoding matrix estimation code, it generates the same symbols for the first antenna, because they has the same first precoding codebook which is $\frac{1}{\sqrt{2}}$. This will help the receiver part to recognise the symbols. For 2nd antenna's symbols, the known precoder matrix index will help the detection process in receiver.

The precoding block system requires 121 clocks cycle to generate a symbol. As for the precoding with OFDM block, it requires 2021 total clocks to generate 1024 bit. Each block of OFDM requires 512 bit inputs. In the system of 2x2 MIMO, it requires 2 OFDM block or 2x512 bit total inputs. The FPGA has maximum clock frequency of 100 MHz, or 10ns in periode. The bit rate for the designed system is:

$$Bit\ rate = \frac{1}{19000\ ns} x\ 3072\ bit\ =$$
$$1616842105.263158 \frac{bit}{second} \approx 161.68\ \text{Mbps}$$

5. Conclusion

The design system has meet the requirement of the desired system. It generates 161.68 Mbps bitrate on simulation and implementation stage with 100 MHz clock frequency. 1% occupied slice, 1% slice register, 1% 4 input LUTs, 27% Bounded IOBs, and 6% BUFG/BUFGCTRLs of FPGA resources are required for the precoding block system implementation. Precoding block system that has been connected to the OFDM block requires 62% occupied slice, 11% slice register, 48% 4 input LUTs, 27% Bounded IOBs, and 9% BUFG/BUFGCTRLs of FPGA resources. The system is succesfully implemented on FPGA Virtex-4 XC4VLX25-SF363 board with above requirement by the help of chipscope software from Xilinx. The implementation shows the same result with the simulation on Isim software.

Although it's already reached the required bitrate for LTE standard, the built system has not perfect yet, because the resource element mapper is not built in this research for the LTE physical layer complete structure.

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